IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A method for planarizing a surface of a semiconductor wafer, comprising [[the steps of]]:

depositing an insulator layer on the semiconductor wafer;

performing a first polishing process on a surface of the insulator layer deposited on the semiconductor wafer while supplying slurry to the surface of the insulator layer; and

performing a second polishing process on the surface of the insulator layer while supplying water to the surface of the insulator layer.

2. (Original) The method of claim 1, wherein the insulator layer is an inter metal dielectric ("IMD") layer.

3. (Original) The method of claim 2, wherein the IMD layer is made of fluorinated silicate glass ("FSG"), undoped silicate glass ("USG"), tetraethoxysilicate ("TEOS") or SiH.

4. (Original) the method of claim 1, wherein about 80% thickness of a total polishing target of the insulator layer is removed by the first polishing process and the remainder of the insulator layer is polished by the second polishing process.